Project Summary

We plan to develop nanostructured materials for interconnect and packaging components that will render unique properties and advantages in future generations of electronic devices. Four basic ideas are proposed; (1) Nano-twinned Cu lines with ultra-high strength and normal conductivity so that they can act as free standing interconnects with air as the lowest k dielectric, (2) Nano hollow particles as low dielectric constant materials for Cu/low k integration, (3) Nano-layered thin films as self-heating under-bump metallization to join Si chips to modules with minimal thermal stress, and (4) improvements in the reliability by control of electromigration degradation of nanostructured interconnects. Both experimental and theoretical investigations are fully integrated in this proposal. In addition, Intel is our industrial partner. Education and research will be integrated by developing two graduate courses on "Mechanical properties of nanoscale structures" and "Kinetic processes in nanoscale structures." International collaboration with Germany, Taiwan, and the Ukraine has been established. The theme of this proposal belongs to "Nanoscale structures, novel phenomena, and Quantum control" and "Multi-scale, multi-phenomena theory, modeling and simulation at the nanoscale" as stated in the Call for Proposals of NSF.

Intellectual Merit

Nano-twinned Cu has ultra-high strength, but its conductivity is as good as coarse-grained Cu. We propose to integrate free standing nano-twinned Cu lines with the lowest k (air); the integration will result in minimal thermal stress. The nano-twinned Cu can also serve as high strength interconnecting columns in packaging technology. We plan to use the Kirkendall effect to produce hollow nanoshells of SiO_2 and Si_3N_4. By sintering, we can obtain a high percentage of porosity in a dielectric film without the limitation due to percolation or the formation of interconnecting pores. Nano-layered under-bump-metallization can provide self and localized heating to achieve chip-join in flip chip technology; again greatly reducing the thermal stress between Si chips and the substrate. An in-situ electromigration study in a TEM will enable us to observe and explore the fundamental phenomena associated with electric current induced plastic deformation, and to assess the reliability of nanostructured interconnect. The multiscale computational approach will serve as a *materials-by-design tool-kit*, and will be integrated with validation experiments aimed at optimizing processing conditions, mechanical behavior and in-service performance. Key features of the modeling effort will include studies for the nucleation of nano-twins, dislocation motion in nano-twinned Cu, dislocation interaction with twin interfaces, effects of electron conduction on dislocation motion and transmission across twinned interfaces, vacancy production by non-conservative dislocation motion, vacancy migration by diffusion and void growth by vacancy condensation under thermal stress and electric current conditions during service, and prediction of the consolidation kinetics of nano particles during sintering.

Broader Impact

The proposed project has direct applications to future nanoelectronic technology. It will expand the applications of nano materials and technology, and enhance the leading position of the US in global competition for markets in electronic devices. Our partnership with Intel will ensure that our findings are not just academic but will benefit the US industry as well. Integration of teaching and research by the development of two new courses for the properties of nanoscale structures will be most helpful to our graduate students, and prepare them for global competition and research. Our close interaction with scientists from Germany, Taiwan, and Ukraine will enable us to exert our influence on their work, to absorb their new findings, and to use their unique equipment.

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C.I. Introduction

Information technology, especially in the microelectronics, has been a major contributor to economic growth and job generation in the U.S. Modern electronic devices are built on semiconductor wafers, mostly silicon wafers. Silicon wafer based integrated circuit devices are the drivers of current information technology. Microelectronic technology starts from a 2-dimensional area on a wafer surface and builds to 3-dimensional device structures. For example, ion implantation is used to dope semiconductors, oxidation to grow interlayer insulators, and a combination of lithography and thin film deposition processes to define the very-large-scale-integration (VLSI) of metallic interconnect conductors. These processes belong to either “Front end of the line” or “back end of the line” using the oxide layer as a divider. The making of millions and now billions of electronic circuits on a chip concerns not only the interaction between an atomic or energy flux and a given wafer surface but also the continuous shrinking of device dimension from micro to nano region. Because of the complexity of the technology and density of integration, device yield and reliability are now intimately connected to materials design, processing, and characterization in the nanoscale domain.

Rapid advances in microelectronic technology have followed Moore’s law, which states that the density of memory and logic circuits on a Si chip will double every 18 months. So far, the prediction has been surprisingly true. By shrinking the linear dimensions of “feature size” of a device, the microelectronic industry has been able to obey Moore’s law by working together and by following the guidelines stated in the International Semiconductor Technology Roadmap. Although Moore’s law does not predict an end, the general believe is that we are getting closer to that end. This is because the industry is approaching several materials limits. For example, the gate oxide thickness is approaching the limit of quantum tunneling, the lithographic technology is approaching the limit in optical wavelength and shift, and the resistance-capacitance delay in interconnects is now a major bottleneck in ultra large scale integration of circuits. Beyond the end of microelectronic technology, we believe the best outcome will be a transition to nano-electronic technology.

How can we make the transition is the most challenging task. Indeed, to produce nano-size device features on a Si wafer is non-trivial. Scaling down from micro-size to nano-size devices requires revolutionary inventions rather than incremental step-by-step improvements. In reality, the probability of success is much better to link the downward path of miniaturization on wafer-based micro-technology with the upward path of a nano-technology. This is because of the existence of a huge quantity of manpower, knowledge and experience that have been accumulated over the past half-century on wafer-based microelectronic technologies. In today’s laboratory environment, the minimum feature size of field effect transistor (FET) device is as small as 7 nm [1]. The challenge is how to integrate a very large number of such small or even smaller transistors and circuits on a wafer. It is reasonable to expect that we may be able to combine today’s Si technology and a new nano-technology to achieve a hybrid technology. In this technology, one of the most important constituents is nanoscale materials science and engineering.

The main goal of proposed work is to investigate processing, properties, and structures of new nano-structured materials for future interconnect and packaging technology. The approach combines experiments and large-scale computational modeling in an integrated and focused way. On the experimental side, we propose to develop three nanostructured materials for interconnect and packaging applications: (1) Nano-twinned Cu lines with ultra-high strength and normal conductivity so that they can act as free standing interconnects with air as the lowest k dielectric, (2) Nano hollow particles as low dielectric constant materials for Cu/low k integration, (3) Nano-layered thin films as self-heating under-bump metallization to join Si chips to modules with minimal thermal stress. We will also conduct an in-situ electromigration experiment in a TEM to observe and explore the fundamental phenomena associated with electric current induced plastic deformation, and to assess the reliability of nanostructured interconnect. In addition, we will develop experimental techniques to (1) non-destructively determine the mechanical properties of the nano-twinned Cu, (2) implement a single on-

line system to pattern and densify the hollow nano shells as the ultra-low dielectric constant interlayer dielectrics, and (3) simultaneously trigger the explosive reaction of nanolayer thin film UBM for filp chip solder joint. The multiscale computational approach [2,3] will serve as a *materials-by-design tool-kit*, and will be integrated with validation experiments aimed at optimizing processing conditions, mechanical behavior and in-service performance. Modeling and simulation will be used to determine how to manage nano-scale plastic flow for optimizing the required high strength without spontaneous failure modes. We will address the question of how to control and manage dislocation motion in small volumes with the intent of designing ultra-strong, high conductivity, and ductile Cu interconnects. The effects of the resulting interconnect microstructure on its ability to conduct both heat and electric current will also be assessed. Key features of the modeling effort will include studies for the nucleation of nano-twins, dislocation motion in nano-twinned Cu, dislocation interaction with twin interfaces, effects of electron conduction on dislocation motion and transmission across twinned interfaces, vacancy production by non-conservative dislocation motion, vacancy migration by diffusion and void growth by vacancy condensation under thermal stress and electric current conditions during service, and prediction of the consolidation kinetics of nano particles during sintering.

Computer-based modeling and simulation of material behavior has become an indispensable tool, and is now playing an increasingly significant role to complement traditional theoretical and experimental research. The main objectives of proposed multiscale modeling efforts are: (1) to guide the experimental processing techniques for optimization of nano-structured materials; (2) to interpret experimental data on the mechanical behavior of nano-structured materials because of the specialized nature of such tests; and (3) to predict in-service performance and reliability of future nano-structured electronics. The main techniques that will be utilized in this project are: *ab initio* density functional theory (DFT), classical Molecular Dynamics (MD), Kinetic Monte Carlo (KMC) simulations, coupled ab initio-continuum Peierls-Nabarro models of twins and dislocation cores, Dislocation Dynamics (DD) in anisotropic multi-layer media, and continuum Finite Element Modeling (FEM) of deformation and failure. These multiscale models will be implemented on two clusters of parallel computers: (1) The ISIS cluster in Professor Ghoniem's laboratory, which contains 200 nodes of AMD processors each at 2-2.4 GHz speed, and the W. M. Keck computational cluster in Professor Kioussis's laboratory at CSUN (see section on facilities). The proposed integrated experimental and computational research is described in Section III.

An important component of the proposed research is the partnership with Intel (see the supporting letter in the Attachment). We will thus have constant input from Intel to guide us to address relevant issues on interconnect and packaging technology. We also believe that education, research, networking, and corporation between US and international countries are essential. To integrate education and research, we will develop two graduate courses at UCLA on " *Mechanical properties of Nanoscale structures*" and "*Kinetic processes in nanoscale structures*." The contents of these two courses are given near the end of this Section. For international interaction, we have in the Attachment, a letter from Prof. Lih J. Chen, Dean of Engineering, National Tsing Hua University, Taiwan, who offers us to use their two latest models of transmission electron microscope in our proposed studies. In addition, we will maintain a close interaction with Prof. Ulrich Geosele, Director of Max Planck Institute of Microstructure Physics at Halle, Germany, on processing of nano materials, and with Prof. Andriy M. Gusak at Dept. of Theoretical Physics, Cherkasy National University, Ukraine, on kinetic analysis of formation and stability of hollow nano particles.

C.II. Background of Proposed Nanoscale Interdisciplinary Research Projects

C.II.1. Nano-twinned Cu as free standing interconnects

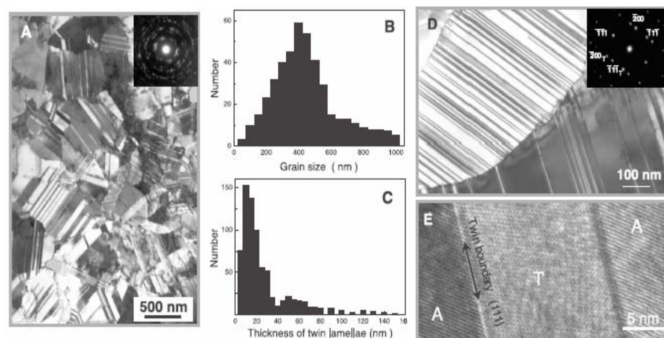

FIG. 1 TEM image of nano-twinned Cu [2]

In a recent Science paper, Lu *et al* reported [4] a fascinating phenomenon that has attracted much attention. Using pulsed electro-deposition technique they synthesized pure copper samples with a high density of nanoscale growth twins, as shown in Fig. 1. The lamella thickness of the twins showed a peak to about 15 nm. The pulsed electro-deposition was carried out galvanostatically using cathodic square wave pulses by turning off the current periodically, with a duty cycle of on-time of 0.02 sec and off-time of 2 sec. The peak current density is very high at about 0.5 A/cm^2 and the pH value in the bath is very low, about 1. The substrate used was amorphous Ni(P), which was also electroplated on an iron sheet. As Fig. 2 shows, the nanoscale twins exhibit a tensile strength about *10 times higher than that of conventional coarse-grained copper, while retaining an electrical conductivity* comparable to that of pure copper. This rare combination will be very valuable as a VLSI interconnect material. The ultrahigh strength will be good for the mechanical properties of the multi-level interconnect structure and also for chemical-mechanical polishing (less dishing) in manufacturing of the dual-damascene structure. Furthermore, it can serve as a candidate for freestanding interconnects using air as dielectric insulation. The major advantage of a free standing interconnect is that there will be no thermal stress between the interconnect and air.

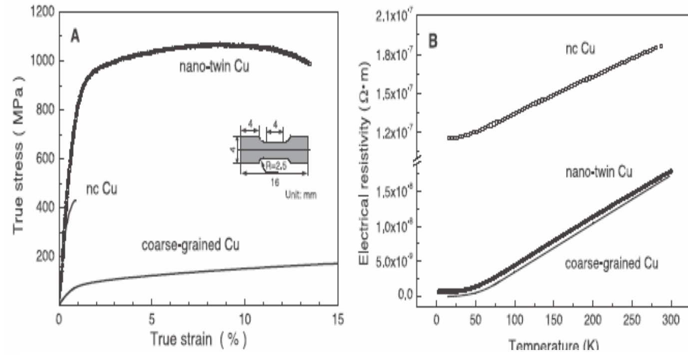

FIG. 2 Mechanical and electrical properties of nano-twinned Cu [2].

C.II.2. Hollow Nano Particles as Low Dielectric Constant Materials in Interconnect and Packaging Technology

There has been recent keen interest in controlling the shape and size and materials at the nanoscale. Nanocrystals, nanorods or wires as well as nanotubes with varying core/shell structures have been fabricated. There is also a deep interest in methods to fabricate hollow nanostructures, especially hollow nanospheres. One intriguing fabrication route recently demonstrated is compound formation in solution, starting from solid nanoparticles of one of the constituents. [5] The formation of a void in the center of the particle is attributed to the Kirkendall effect [6, 7] associated with different diffusion rates of atoms moving in and out of the sphere. An example of hollow nanocrystals of CoO s shown in Figure 3. [5]

The Kirkendall effect was originally observed in bulk diffusion couples of Cu and CuZn [6].To apply the Kirkendall effect to form hollow nanostructures, it is more sensible to choose a diffusion couple, which forms a compound rather than solid solutions as in the Cu/CuZn case. In this case, one of the reactants is a spherical solid particle of "A" and the other reactant "B" may be supplied from a gas or liquid phase or by a solid shell of B around the core particle of A. The resultant compound $A_\alpha B_\beta$ forms between A and B, as for example, in the case of silicide formation, i.e., $2Ni + Si \rightarrow Ni_2Si$. In solid/solid nanosphere reactions, A and B may interchange as core and shell, e.g., both a nickel-coated silicon core and a silicon-coated nickel core are possible starting

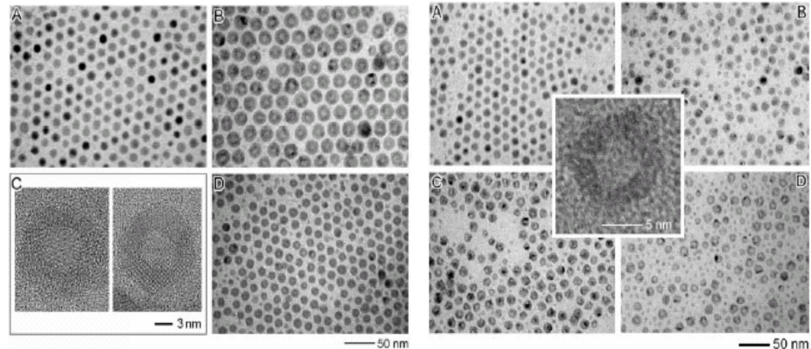

FIG. 3 Hollow nanocrstals of

configurations. It is obvious that the formation of an empty core will only occur if the out-diffusion of atoms is faster than the in-diffusion. In silicide formation, there are cases in which the metal is the main diffuser (as in Ni_2Si), so the core has to be metallic in order to form hollow silicide structure. There are also silicides in which silicon is the main diffuser, so the starting core should be silicon as in the case of WSi_2 formation.

If we turn to gas reactions and restrict ourselves to silicon cores again, it is obvious that the oxidation of Si particles in oxygen atmosphere will not lead to hollow SiO_2 spheres since oxygen diffuses in. [8]. In contrast, nitridation of a solid silicon sphere should lead to a Si_3N_4 hollow sphere since silicon is moving out faster than nitrogen is moving in, by judging from the thin film case in which nitridation of silicon leads to vacancy injection. [8]. Instead of compound formation, a dissociation reaction with appropriate diffusion fluxes may also lead to hollow spheres. It is well known that at high temperatures, the reaction of $Si + SiO_2 \rightarrow 2SiO$ is predominant in the absence of O_2. [9] This is why thin SiO_2 layers on silicon wafers evaporate in MBE reactors above about 900°C, which is used for generating clean silicon surfaces. Therefore, an oxidized silicon core annealed in vacuum should show the generation of SiO, which diffuses out of the SiO_2 shell, consuming the Si in the core, and leaving an empty SiO_2 shell.

The advantage of nanoshell of SiO_2 is that by sintering we can produce a porous SiO_2 thin film having a high percentage of porosity without interconnecting pores. It is known that the porous zero-gel or aero-gel SiO_2 thin films fabricated by the sol gel method cannot exceed the 18 % porosity limit, the percolation limit, without the formation of interconnected pores. Hence, even if we use a carbon doped SiO_2 with a dielectric constant of around 3, we can only reduce it to about 2.4 by adding pores using the sol gel method. If we use nanoshells of SiO_2, we can surpass the percolation limit. On the other hand, the thermal stability of hollow nanoshells should be considered. We expect that a hollow nanoscale particle may not be thermodynamically stable at high temperatures; it will shrink and transform to a solid nano particle. Nevertheless, hollow nano SiO_2 particle will be stable to the device operation temperature near 100°C. If helium atoms are implanted into these hollow nano-spheres, a central bubble can be formed, and the upper temperature for the stability of such hollow nano-spheres can be greatly increased.

C.II.3. Nano multilayer under-bump-metallization (UBM) thin films as self-heating sources for flip chip solder joints in electronic packaging

The microelectronic industry has been using an array of solder joints to connect the very-large-scale-integration of circuits on a Si chip to a substrate. By using a process called “reflow,” the solder bumps on a Si chip are joined to the bond pads on the substrate in a furnace at a temperature slightly above the melting point of the solder. Owing to the difference in thermal expansion coefficient between the Si chip and a polymer-based substrate, there exists a large thermal stress between the chip and the substrate after cooling down from the reflow. The thermal stress is a serious problem and a reliability concern when the Cu/low k technology is to be introduced into the Si technology. This is due to the large thermal stress between the Cu and the low k material. When the chip-to-substrate thermal stress is added to the stress in the Cu/low k, the devices will have very poor yield and reliability. At the moment, thermal stress is the most challenging problem in processing Si devices.

We can replace the reflow process by a *novel* process of self and local heating to achieve solder joints. Because of local heating, there is much less thermal stress between the Si and the substrate. In other words, we do not need to heat the whole Si chip and the entire printed circuit board in achieving solder joints, as in a reflow process. It has been reported that in multi-layered bi-metallic thin films of Al and Ni, i.e., a structure of alternating layers of Al and Ni thin films of thickness in the nanometer range, an explosive reaction occurs [10-12]. For example, when we prepared about 20 layers of Al/Ni/Al/Ni/Al/Ni, in which the thickness of Al and Ni is 10 to 30 nm, we can induce an explosive reaction in the multi-layered structure by a small impact. The explosive reaction is due the rapid release of chemical energy of the formation of an intermetallic compound between the nanolayers of Al and Ni. The reaction becomes self-sustained and it propagates rapidly through the entire film by self-heating. The reactive

multiplayer foils are also available through Reactive Nano Technologies (Hunt Valley, MD) for soldering and joining.

We plan to fabricate the under-bump-metallization (UBM) or the bond pad by using a multi-layered bi-metallic thin film structure of nano-thickness. UBM is the metallization on Si where the solder bump is placed, while bond-pad is the metallization on the substrate where the solder bump is to be joined. There are many options in chip-join, i.e., to join electrically a chip to its module or substrate. Here we take a composite solder joint for illustration. In using composite solder joints, an array of high-Pb (97Pb3Sn) solder bumps has already been reflowed on a Si chip. On the substrate, there are already eutectic a solder pedestal (flattened surface) on the bond pad. In conventional processing, the Si chip is flipped over so that the high-Pb bumps are placed one-to-one on the eutectic solder pedestals and followed by a reflow to join them together. The challenge is how to replace the reflow by self-heating to achieve chip-join. Several approaches will be developed to trigger the explosive reaction of nanolayer thin film UBM for flip chip solder joints.

C.III. Proposed Nanoscale Interdisciplinary Research Project

C.III.1. Nano-twinned Cu as free standing interconnects

a. Processing of nano-twinned Cu

At UCLA, we have designed and built an electro-plating bath with a pulsed constant voltage source to explore the deposition of nano-twinned Cu (in collaboration with Semiconductor Research Corporation). The details of the electro-plating procedure from an electrolyte of $CuSO_4$ were not described in ref. [4]. Up to now, our attempts have enabled us to gain much understanding of the pulsed electro-plating process to produce nano-twinned Cu. We are currently optimizing the plating condition to obtain a very high density of nano-twins in Cu. We found that, to produce nano-twinned Cu by pulsed electroplating, we have to control and optimize the following six parameters: (1) Composition of the plating bath is $CuSO_4$, yet we must increase the anion concentration or the ionic conductivity by adding $NaSO_4$. In addition we must add a buffer (typically boric acid) to control the pH level; (2) The pH level is 1 which is very low, so it is a highly acidic bath; (3) Temperature will be near room temperature; (4) The current source will be a pulsed DC source preferably a squared current pulsed source with a very short on-time of 0.02 sec and a very long off-time of 2 sec or more. The current density will be very large; (5) Agitation will be required, preferably a rotating electrode rather than the use of mechanical stirring by a magnet, and (6) Some additives might be needed such as a lever agent (large molecules) to achieve conformal deposition in trenches, and a brighter to smooth the surface topology.

Clearly, the high-pulsed current density and the very low pH are to enhance the nucleation of twins. The high density of twin nucleation will require a diffusion-controlled deposition rather than an interfacial reaction controlled deposition. The very short on-time pulse will allow us to apply very high peak current density to enhance nucleation, and the long off-time will allow ionic diffusion in the bath to occur. The agitation will enhance the uniformity of deposition. If we apply a high current continuous DC source in a low pH bath, we will obtain a nano-grain and porous film. Also, we should mention that TaN and TiN have large surface free energies, which will enhance the rate of heterogeneous nucleation of Cu. While much still has to be done to optimize the deposition process, we are confident that we will be able to reproduce the deposition of nano-twinned Cu on a flat surface coated with TaN or TiN and in dual damascene structures.

b. Mechanical behavior of nano-twinned Cu

We will study the mechanical properties of the nano-twinned Cu, including yield strength, true stress-true plastic strain curve, and tensile strength and creep behavior. Both conventional destructive testing and a new nondestructive testing technique based on automated ball indentation (ABI) will be used. The localized ABI test is non-destructive and can be used in-situ to measure the stress-strain properties. The stress-strain curve measured with the ABI test has been demonstrated to correlate with the stress-strain curve measured in a tensile test [13-14] In the ABI test, a spherical (ball) indenter with a diameter of 25 μm is forced into the surface of the nano-twinned copper. The spherical shape of the

indenter causes an increasing strain with increased indentation depth to a maximum of 20% true plastic strain. A true strain of 20% corresponds to a penetration depth equal to the indenter radius. The penetration depth of the spherical indenter into the test surface is measured with a spring-loaded linear variable differential transducer. The force required to indent the material to increased depth values is measured with a force transducer such as load cell. Periodic partial unloadings during the test are used to determine the elastic strain. The elastic strain is subtracted from the total strain to give the plastic strain. The incremental values of the ABI-measured true stress and true plastic strain are calculated from the indentation force-depth data. The ABI-derived yield strength is determined from the force-depth data. Several properties including the strain-hardening exponent, uniform ductility and ultimate tensile strength may also be estimated from the ABI test. The entire test is fully automated (computer controlled), where the spherical indenter is driven into the test specimen at a desired speed, thus controlling the strain rate of the ABI test.

For conventional destructive testing, miniaturized dog-bone specimens will be used. Tensile specimens will be electro-polished to prevent premature failure due to the pre-existing surface flaws. Uniaxial tensile tests will be performed in an Instron universal testing machine at different strain rates. The fracture characteristics will be examined using a scanning electron microscope. Both creep and stress relaxation characteristics of nano-twinned copper will also be determined using the ABI test equipped with either a spherical indenter or a flat-end cylindrical indenter. During indentation creep testing, the stress is held at a constant value and the indentation creep strain is monitored for the desired duration of the test. For the indentation stress relaxation test, the strain is held constant and the indentation stress relaxation is monitored. The load, depth, stress-versus time and strain versus time will be recorded automatically during the test. The mechanisms of creep deformation will be elucidated using a transmission electron microscope.

c. Modeling and simulation of nano-twinned Cu

Two of the most common and important modes of plastic deformation in fcc metals at low temperatures are slip and deformation twinning (DT). Slip is propagated through dislocations while deformation twinning occurs when a region of crystal is transformed by the external loading into its twin (mirror) counterpart. The likelihood of a material to twin, as opposed to slip, is referred to as its twinnability [15]. Recently, pure copper samples with a high density of nanoscale growth twins showed a tensile strength about ten times higher than that of conventional coarse-grained copper, while retaining an electrical conductivity compatible to that of pure copper [16]. Experimental observations have shown that a low intrinsic stacking fault energy (SFE) is correlated with a higher tendency to twin in fcc metals [17]. It has also been suggested experimentally that the SFE of the metal will have to be less than some critical value for a metal to exhibit deformation twinning [17]. Twins prefer to nucleate at grain boundaries (GBs) to reduce the grain boundary energies by means of the twinning-induced orientation change. The formation of twins depends strongly on the ratio of the twin boundary energy, γ_{TB}, to the GB energy, $\alpha = \gamma_{TB} / \gamma_{GB}$. Large twins densities may be obtained in metals with smaller α values [16]. Another important micro structural parameter influence deformation twinning is the grain size in the metal. It has been reported that increasing the average grain size results in a lower twin nucleation stress for a given metal [17].

Experimental results and isotropic elasticity estimates show that the dominant mechanism that controls the strength and hardness of multi-layer thin films is the influence of the dislocation image force associated with a mismatch in elastic properties between adjacent film layers [18]. For layered materials with a large mismatch in elastic properties, a significant hardness enhancement was observed [18,19]. Two models are often used to explain the observed behavior of hardness (or flow stress) in thin films. In the threading dislocation model [20,21], the flow stress is determined by the energy balance between the threading glide dislocation segment and the misfit dislocation left behind at the interface. This model results in a flow stress that scales approximately with the inverse of the film/layer thickness. In this model, interfaces are introduced as impenetrable planes for dislocations. The second model is an extension of the well-known Hall-Petch effect. Here, dislocations are assumed to form a pile-up at a

boundary until a critical stress is reached. This results in a flow stress, which is inversely proportional to the square root of the layer thickness or grain size. Both models qualitatively explain the increase in the flow stress with decreasing film/layer thickness, but not the behavior as the layer thickness decreases below tens of nano-meters.

As individual layers become very thin (i.e. in the tens of nanometers), only single dislocations can propagate and expand upon the application of an externally applied stress. However, because the layer thickness is very small, the curvature of the dislocation loop in segments subtended between layers would be extremely high, and thus self-forces in these regions are very substantial. The externally applied stress would have to overcome such large self-forces if these curved segments are to expand. The applied P-K force on those segments that are parallel to the interface does not have to overcome self-forces because the curvature of these segments is small. Rather, the image force from neighboring and other interfaces would have to be overcome by the applied P-K force. Since we regularized the solution by selecting a cut-off radius of one Burgers vector on either side of the interface, the dislocation will be repelled with a maximum image force on one side of the interface, and then attracted with a different maximum force once it crosses the interface. If the applied stress is high enough that the maximum P-K force on the straight dislocation segments close to the interface overcomes both repulsive and attractive forces, the dislocation will cross from one layer to the neighboring one, and Confined Layer Slip (CLS) is finally lost.

The main issues that we plan to address here are:

1. Nucleation of nano-twins;
2. Dislocation motion in nano-twinned Cu,
3. Dislocation interaction with twin interfaces; and
4. The effects of electron conduction on dislocation motion and transmission across twinned interfaces.

To understand these four areas, which control the mechanisms of twin formation and subsequent plastic deformation and strength, we plan to pursue a multiscale modeling strategy, as outlined below.

- We will use ab initio calculations to determine the *multiplane* generalized stacking fault energy surface [22] (GSFES), which describes the energy penalty incurred when an arbitrary number of planes, n+1, are *sheared* relative to the adjacent plane by a common displacement, **x**, that lies in the slip plane. In our previous calculations [23,24] of the dislocation core properties in aluminum we have calculated the GSFES for shearing only two adjacent planes.
- We will use ab initio calculations to determine the generalized stacking fault energy surface for various twin boundaries, which describes the energy penalty incurred when a twin boundary is displaced.
- We will extend the Peierls-Nabarro (PN) model to twin boundaries. This model provides a link between continuum elasticity and atomistic simulations [23-26] In our previous work; the atomic rows were confined to above and below the glide plane. We are currently generalizing the model to study the interface between two dissimilar materials.[9] For the case of twins, the PN model needs to be extended so that the displacement field is allowed to spread both in the slip (-111) plane and the twin boundary (111). We will study the dislocation core properties for edge and screw dislocations. These will include the core width, the Peierls stress, i.e. the critical stress to propagate the dislocation across the twin, the effect of dissociation. For example, it has been argued [16] that the ½[01-1] dislocation would propagate across the twin, whereas the motion of ½[110] and ½[101] dislocations would be blocked at the twin boundary.
- We will employ dislocation dynamics for *3D dislocation loops* of arbitrary geometry interacting with a TB. The *nov*el feature of such calculations will be to include the lattice restoring force determined from the ab initio calculations described above. We have recently applied this novel method to determine the core structure in aluminum [27]. The computational *continuum-atomistic hybrid model* would help understand for the first time the nucleation of dislocations from twin boundaries.

- We will also employ classical Molecular Dynamics (MD) simulations based on empirical potentials (such as the Mishin potential) to determine the critical forces required to propagate dislocations across twin interfaces. Our recent results indicate that dislocations in nano-laminate Cu dissociate into partials as in bulk materials. However, the width of the stacking fault and the dislocation velocity are strong functions of the laminate width [28]. While the leading partial can cross a nano-laminate interface, the trailing partial can be impeded for a long time, and the dislocation core can spread over many nano-laminates. We will investigate this interesting behavior of dislocations in nano-twins. The ability of dislocations to cross twin boundaries will ultimately determine the maximum attainable strength.

Since elastic anisotropy is an important factor for the deformation of Cu, we extended our original work on Parametric Dislocation Dynamics (PDD) to fully anisotropic crystals [29,30]. Efficient computational methods for the elastic field, self and interaction forces of 3-D dislocations in anisotropic elastic crystals are developed for incorporation into dislocation dynamics computer simulation codes. The elastic field of a general dislocation loop is determined by incorporating numerically-evaluated derivatives of Green's functions in the fast sum method of Ghoniem et al. [31]. High numerical accuracy and computational efficiency of the method are demonstrated. Self-forces of dislocation loops are calculated by numerical integrations performed on the dislocation line, and several approximation methods to the full integration are also explored. The effects of elastic anisotropy in cubic crystals on the elastic field, self-forces, Frank-Read source expansion, finite-length dipoles and dislocation junctions are systematically determined. Large-scale 3-D dislocation dynamics simulations are carried out with full elastic anisotropy in Cu single crystals. We found that the dislocation microstructure and strain hardening behavior are strong functions of elastic anisotropy [30].

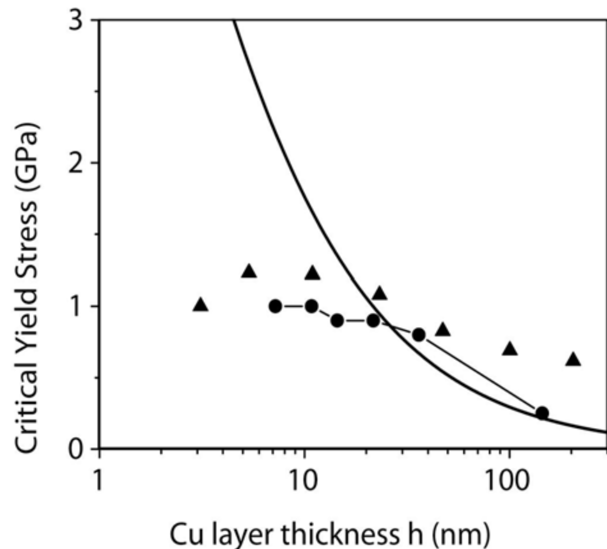

Figure 4 Yield strength of a Ni-Cu layered thin film as a function of the layer thickness. Solid line: Freund's formula, triangles: experimental results [18], and circles: current simulation results

Utilizing Fourier Transforms, we developed numerical methods to determine the elastic field of 3-D dislocation loops in anisotropic multilayer materials [32]. Green's functions and their derivatives, were obtained first in the Fourier domain and then in the real domain by numerical inversion, and then used in both surface and line integrals to determine the elastic field of dislocation loops. The interaction forces between dislocations and free surfaces or interfaces in multilayer thin films were then investigated. The developed method is based on rigorous elasticity solutions for dislocations approaching to within 1-2 atomic planes from the interface. For a dislocation in one layer, the interface image-force is determined mainly by the elastic moduli and thickness of neighboring layers. When a dislocation approaches an interface between two layers, within 10-20 atomic planes, the image force changes rapidly. Our model showed that when a dislocation crosses an interface from a soft to a hard layer, additional external forces must be applied to overcome an elastic mismatch barrier. The developed method extends the concept of the Kohler barrier in 2-D, and shows that the interface force barrier not only depends on the relative ratio of the elastic moduli of neighboring layers, but it also depends on the 3-D shape of the dislocation, the number of interacting adjacent layers, and on layer thickness. Figure 4 shows results of our calculations for the maximum strength of a copper layer in a thin film of alternating Cu/Ni layers based on the activation of a single F-R source, as a function of the

layer period. Experimental results for nano-indentation by Misra et al. [19] and Clemens et al. [18] are also shown. Since Freund's formula [20] is often used to estimate the strength of thin films, film strength using this formula is also shown as a solid line on the same figure for comparison. For layers of thickness less than approximately 100 nm, a single F-R source will determine the overall strength of the layer as a competition between confinement in the layer by image forces generated by elastic modulus mismatch, and resistance to deformation by self-forces on the curved ends of the dislocation loop. If the modulus mismatch is not too great, dislocation loops will cross from layer to layer rather than be confined within a layer. One would expect that the maximum strength be determined by the layer thickness and the ratio of elastic modulii as well. For thicker layers, F-R sources can operate many times leading to dislocation multiplication and the formation of a pile-up. In such case, the dominant deformation mode is the Hall-Petch mechanism. Currently, there are no estimates in the literature for the critical stress required to push dislocations across twinned anisotropic interfaces, such as the case with nano-twinned Cu. We plan to extend our work in nano-laminated anisotropic thin films to determine the critical yield stress for nano-twinned Cu. A few new aspects must be considered in our study, as discussed below.

1. Since Cu is elastically anisotropic, the elastic compliance tensor will have to be described in a common coordinate system, and thus we would have significant changes in elastic anisotropy as dislocations cross from one twin lamella into a neighboring one. The methods that we developed for multilayer anisotropic thin films will be employed here as well [32].
2. A dislocation array model for twin boundaries must also be incorporated in our simulations [33,34]. As dislocation loops expand inside the twin, they will interact with the twin boundary that is represented by two dislocation arrays at the top and bottom interfaces.
3. When an external stress is applied, de-twinning may be a possibility as a result of twin boundary motion. The migration of twin boundaries and the simultaneous interaction with lattice dislocations will be investigated.

C.III.2. Hollow nanospheres of SiO_2 as ultra-low k dielectric

a. Processing of hollow nanoshells of SiO_2 and Si_3N_4

To process hollow nanoshells of SiO_2, we start with Si nano particles and oxidized them partially to obtain solid particles having a core of Si with a coating of SiO_2 over it. Next we shall annealing them in ultra high vacuum, the Si in the core will diffuse out to reaction with the SiO_2 coating to form SiO, but in ultra-high vacuum, the SiO is unstable and evaporate away. Thus, we will obtain nanoshell SiO_2. To control the diameter and thickness of the nanoshell, we will perform systematic experiments to determine what will be the initial size of the nano Si and how thick is the coating of SiO_2 so that we can control the percent of porosity of the film when the nanoshells are sintered together. Also we will anneal the nanoshells in carbon ambient to see if we form carbon-doped nanoshells. To process hollow Si_3N_4, we shall nitridize Si nano particle in nitrogen. Again, a systematic study will be performed to control the diameter and shell thickness of the hollow nano Si_3N_4 particles.

b. Sintering Characteristics of Hollow Nanoshell SiO_2

We will develop a single on-line system to pattern and densify the hollow nano shells as the ultra-low dielectric constant interlayer dielectrics (ILD). Initially the hollow nanoshell SiO_2 will be dispersed in a solvent to form a solution. The solution containing hollow nano SiO_2 particles is fed to an inkjet nozzle that generates a software-controlled pattern on a substrate. Subsequently, the colloids are exposed to an intense laser beam that leads to drying and densification to form a nanoporous ceramic. The use of laser heating to densify nano-sized SiO_2, TiO_2 and SiO_2-TiO_2 ceramics and thin films has been reported in the literature [35,36]. However, laser heating enables a rapid densification of nano-sized ceramic powders to suppress the excessive grain growth during sintering.

The microstructure and morphology of the sintered nanoporous SiO_2 will be thoroughly characterized using scanning and transmission electron microscope. The thermal stability of hollow nanoshells at elevated temperatures will be analyzed. The shrinkage induced during laser sintering

process will be quantified to provide input for modeling the sintering process of nanoporous ceramics. The porosity content and pore size distribution in the sintered nanoporous SiO_2 will be analyzed. The influence of laser power density, the fluence and the interaction time on the densification of nanoporous ceramics will be investigated. The dielectric properties of the resulting nanoporous SiO_2 will be determined. The mechanical properties of the sintered nanoporous SiO_2 will be determined using a nano-indentation technique. The Young's modulus and hardness will be measured using an MTS nanoindenter XP.

c. Kinetic analysis of stability and formation of hollow nano particles

A general method of obtaining hollow nanoparticles by utilizing the Kirkendall effect has been reported recently. [5]. We have examined the thermal stability of hollow nanoparticles of a pure element [37] since it is relatively easy as compared to the formation of hollow nano particles by interfacial reaction. Hollow nano particles are intrinsically unstable. The proposed mechanism of instability is the vacancy flux going from inner surface (with radius r_i) to external surface (with radius r_e). The driving force of vacancy flux is the difference of vacancy/atoms chemical potentials and corresponding difference of equilibrium vacancy concentrations at the two curved surfaces, $C_V(r_i) > C_V(r_e)$. The difference will generate out-flux of vacancies and transform the hollow nano particle to a solid nano particle. It has been shown that the time, t, needed to transform a hollow nanosphere of Au of 5 nm to a solid Au nanosphere at 400 °C will be only a few seconds. [37].

To analyze the instability and shrinking kinetics of nanoshells of an alloy or intermetallic compound is much more complicated. Following the classic Darken's analysis of interdiffusion, we will have to add Gibbs-Thomson effect into the analysis. Also we will use kinetic Monte Carlo simulation to analyze the stability issue. To analyze the kinetics of formation of nanoshells by interfacial reaction and the Kirkendall effect is even harder. We shall extend the thin film reaction having planar interfaces [38] to the reaction of a solid nanosphere of element A with a coating of element B to form an intermetallic compound of AB in between them. Again the Gibbs-Thomson effect must be included. One of the challenges is phase selection from several of the intermetallic compounds, which can be formed between A, and B. We shall consider diffusion-limited process first and then combine it with interfacial-reaction-limited process.

C.**III.3. Nano multilayer thin films as self-heating source for flip chip solder joint**

a. Explosive reaction of nanolayer thin film UBM for flip chip solder joints

To design a nanolayer thin film solder joint as a heating source for flip chip solder joint, we shall keep the high-Pb bump on the Si side without change. On the substrate side, we shall use thin film deposition to deposit first a multiplayer of Al/Ni as bond-pad and follow by depositing a thick layer (about 10 μm) of pure Sn on the multiplayer Al/Ni. For example, we can use immersion Sn. Then we'll flip the Si chip and place the high-Pb bumps on the Sn surface. Next, we will trigger the explosive reaction in the Al/Ni layers and the heat generated will melt the Sn to achieve chip-join. Our effort will be focused on how to trigger the explosive reaction in flip chip configuration. Three different approaches will be used to trigger the explosive reaction in nanolayers of Al/Ni: joule heating due to current crowding, microwave-assisted ignition, and liquid electrolyte.

Due to the unique configuration of a flip chip solder joint, there is a unique phenomenon of current crowding. [39]. When the current enters the solder bump from the Al or Cu interconnecting wire, there is a high degree of current crowding at the point where the current enters the bump because of a very large change in the cross-section (a change of two orders of magnitude) between the wire and the bump. Due to current crowding, the joule heating there is very high and we can use this joule heating to trigger the explosive reaction in the UBM. We can control the explosive reaction by controlling the number of layers and thickness of the layers in the UBM. When we design a daisy chain of solder bumps, we can ignite a serial of joints by passing electrical current. By reversing the direction

of electric current, we can control the point of the current crowding in the solder joints. However, in a real device, we cannot do so since many of the solder joints are isolated. On the other hand, we can use microwave heating to ignite the reaction in the nano-structured UBM. The use of microwave heating to initiate combustion synthesis of various inorganic materials has been successfully demonstrated. Microwave heating. The microwave-assisted ignition approach, if successful, can be implemented in the production line to join thousands of solder ball simultaneously. Finally, we will use liquid electrolyte to trigger the reaction. The advantage is that we can apply the liquid electrolyte as we apply underfill in a flip chip and then we can wash it clean afterward as we wash clean the residue flux in a flip chip.

We will analyze the microstructure of the solder joints formed by reactive multiplayer thin film UBM using a scanning and transmission electron microscope. The adhesion and bonding of solder ball with the reactive thin film UBM will be characterized and compared with those obtained from conventional solder reflow process. The thermal fatigue life of the solder joint formed by reactive multiplayer thin film UBM will also be investigated.

b. Ab initio modeling on energy release

We will employ *ab initio* electronic structure calculations to investigate the energy release during the formation of the multiplayer Al/Ni, as a function of the periodicity of the multilayer system. The energy release will be calculated from the difference of the total energy of the multilayer Al/Ni and the total energies of the individual Ni and Al thin films. The calculations will also explore the effect of the Sn layer deposited on the multilayer on the energy release. We will also calculate the adhesion properties of the multiplayer Al/Ni and the effect of the Sn layer on the adhesion properties.

C.III.4. Reliability and electromigration degradation of nanostructured interconnect

The most common failures in metallic interconnects are related to electromigration, which is the mass transport of a metal due to the momentum transfer between conducting electrons and metal atoms. Electromigration causes failure in microelectronic components by creating voids, which eventually cause open circuits, and hillocks, which can cause short circuits depending on the metallization geometry, and the proximity of metal lines to one another. In the simplest case, void formation is strongly dependent on current directions, and voids will appear near the cathode, while sometimes hillocks can be found near the anode. As device features reduce in Ultra-large-scale integrated circuits, current densities increase with the metallization layer complexity. These issues make understanding Electromigration (EM) induced failure essential to design more reliable circuits. In state of the art metallization systems, electromigration becomes noticeable when current densities approach 10^6 A/cm^2. The activation energies for electromigration in Cu are strongly dependent on process variations, so while the "good" Cu metallization systems will show activation energies over 1 eV , these can also be 0.6 eV and lower, which is actually worse than in state of the art Al.

a. Electromigration of twin boundaries and dislocations in Cu and Sn

The influence of electromigration on plastic deformation is important, because it is known that a high current density may enhance or retard the rate of plastic deformation. At a high deformation rate, if the electrons surrounding a dislocation exert a drag force, the rate is retarded. The applied critical force to move a dislocation is related to the Peierls-Nabarro stress. It also depends strongly on the angle between the current flow direction and Burgers vector of dislocations. However, no direct observation of dislocation motion under electromigration has been reported and the fundamental nature of the interaction has not been studied. The simple picture of the electrical force on dislocation per unit length is that of Huntington's electron wind force; it is proportional to the ratio of resistance of a unit length of the dislocation and that of a lattice atom.

To conduct direct observations of dislocation and twin migration (its migration occurs by dislocation motion along the incoherent twin boundary) under electromigration, we will need a stage in an electron microscope that enables us to apply electric current and heat to the sample. Such an electron

microscope is available in the Department of Materials Science and Engineering at National Tsing Hua University in Hsinchu, Taiwan. The electron microscope has been set up to do in-situ electromigration in Cu interconnect by Assistant Prof. Chien-Neng Liao, who is one of the PI's (K. N. Tu) former Ph. D. students. [40]. The Dean of the Engineering School of National Tsing Hua university, Prof. Lih J. Chen, has agreed to let us use the microscope to conduct the in-situ electromigration studies proposed here. An official letter from Prof. Chen is included in the attachment of this proposal. We intend to measure the threshold current density needed to move a dislocation or a twin boundary, whether it moves towards cathode or anode. We shall study the mechanism of its motion.

Both large grain polycrystalline Cu films and nano-twinned Cu films will be studied. Sample preparation for in-situ TEM observation of electromigration in Cu is not trivial. While the procedure to prepare Cu thin films stripes for in-situ TEM and electromigration study is available, we need to prepare nano-twinned Cu thin film samples for in-situ TEM studies. How dislocations interact with the twins under electromigration will be studied experimentally. To study twin and dislocation migration in Sn under electromigration, we will use Sn lamellae sample and add electrodes so that we can perform in-situ TEM and electromigration study. Figure 5 and 6 are bright field TEM images of the motion of a group of dislocations along the incoherent twin boundary of a twin in a Sn lamella. [41,42] Since the Sn lamellae have surface oxide, the oxide may provide certain pinning force to the dislocations, and the motion of a dislocation will leave a ghost image on both sides of the oxide of the lamellae. Therefore we can observe dislocation motion quite easily. Perhaps this will enable us to observe and explore the basic process in electric current induced plastic deformation [43], as discussed below.

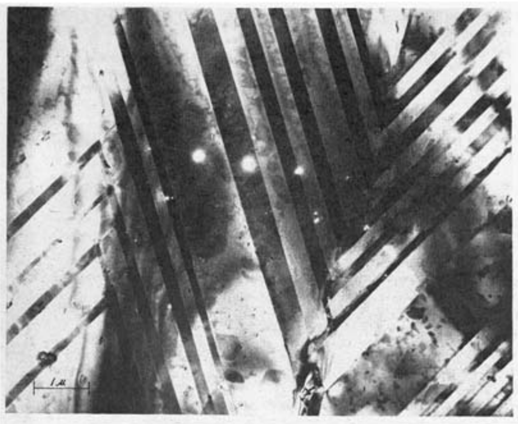

Figure 5 TEM image of incoherent nano-twins in Sn

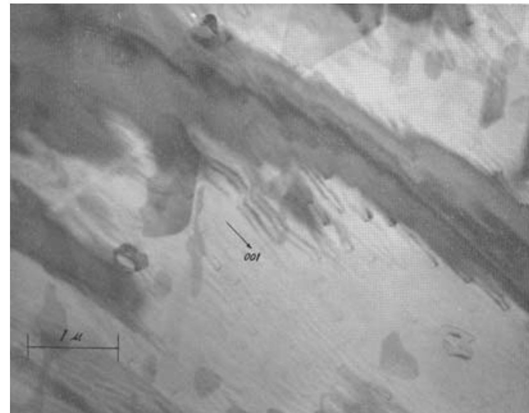

Figure 6 The dislocations were moving along the [110] direction of Sn.

b. Modeling and Simulation of Electromigration

For conducting materials in microelectronics, high electrical conductivity and high mechanical strength are often required simultaneously. However, pure metals with high conductivities such as Ag, Cu and Al are very soft. All present strengthening approaches, which are based on the introduction of various kinds of defects (e.g. grain boundaries, dislocations and point defects) or precipitates, also increase the scattering of conduction electrons at these defects, thus increasing the electrical resistivity.[2] The key to making strong but conductive metals is to find an appropriate microstructure in which dislocations motions are effectively blocked while the scattering of conduction electrons is minimized. The recent experiments of pure copper samples with a high density of nanoscale growth twins showed a tensile strength of about ten times higher than the conventional coarse-grained copper, while retaining an electrical conductivity comparable to that of pure copper. We propose to study the effects of electromigration on interconnect failure using a multiscale approach

Electron Wind Force:

We will apply first principles electronic structure calculations to study in Cu or Sn the electromigration wind force of: 1) Dislocation; 2) Twin Boundary; 3) The Cu/Sn interface; and 3) Sn impurities in the Cu host. We will calculate the driving force $\mathbf{F} = \mathbf{F}_{dir} + \mathbf{F}_{wind} = Z^*eE$, where the direct force is due to a net charge on the migrating atom, while the wind force is due to scattering of the current-carrying electrons off the atoms, and the effective valence Z* is the measurable quantity. To date ab initio electronic structure calculations of electromigration effects have been mainly restricted to metallic bulk calculations or impurities (such as vacancies or alloying elements) in metallic bulk. [11,12] Since dislocations or twin boundaries facilitate diffusion like pipes they should affect strongly the scattering of the electrons by the migrating atoms and hence the wind force. The proposed calculations will reveal whether the reduced electronic charge density along the twin boundary will lead to a reduction of the wind force at the twin boundary or along the dislocation line. The proposed calculations will investigate whether the diffusion of a few percent of Sn atoms at the Cu/Sn interface or the interface itself or the twin boundary can reverse the direction of the flux of host Cu atoms under certain conditions. This flux reversal can slow down electromigration mass transport at the interface considerably, thus driving the electromigration process in the bulk, as is experimentally observed.

Vacancy Generation, Transport & Clustering

Tensile regions in thin metal lines will have higher chemical potential than unstressed or compressive regions. Hence, excess vacancies will be generated in tensile regions. These vacancies may condense to form vacancy loops and/ or void embryos, and compete for capture of additionally generated vacancies. Also, small voids can be transported in the stress gradient set up within the interconnect, and if they coalesce, they may become immobilized. The most significant problem is the formation of at least one single void across the interconnect that increases the resistivety in an uncontrolled manner. The process of Hillock formation is less understood as compared to its counterpart: void formation. The driving force for the formation of Hillocks is a state of compressive stress, especially bi-axial. However, the exact mechanism is either by mass transport in a stress gradient similar to the Nabarro-Herring creep mechanism, or by dislocations punching through the surface to form an extrusion, similar to fatigue induced surface extrusions. In any case, the biggest unknown is why do they form in a localized fashion, rather than relieving the compressive stress by uniform distortion of the surface. Their presence leads to short circuits (unlike voids, which lead to open circuit), and are thus considered very harmful to circuit reliability.

The quality of the Cu/oxide interface, with respect to its ability to act as a diffusion pathway is sensitive to interface conditions, which will most likely have a significant effect on diffusion. It is essential that a careful kinetic study be performed to insure that the surface or metal/oxide interface has been shut off as a diffusion pathway. If testing shows that the activation energy for failure is low, on the order of 0.7 to 0.8 eV, a high diffusivity interface is providing mass transport. If the activation energy is higher, on the order of 1.2 eV or higher, mass transport is proceeding either via grain boundaries or some other more diffusion resistant interface. These differences in activation energies (about 0.5 eV) can mean orders of magnitude differences in time to failure.

To address these issues, which are critical to the reliability of nano-twinned Cu interconnects, we will develop multiscale models of the following phenomena:

1. Vacancy production by non-conservative dislocation motion in the bulk, or at interfaces;
2. Vacancy migration by diffusion in bulk and at interfaces;

Void nucleation and growth under thermal stress and electric current conditions,

Integration of the developed models with our experiments will allow optimization of the interconnect system for greater in-service reliability. Ab initio calculations will be employed to investigate the vacancy formation and migration energies, the migration path on the Cu surface and the Cu/Sn or Cu/ Si_3N_4 interface. These calculations will reveal whether the presence of the Sn overlayer will suppress the formation of vacancies and hence inhibit electromigration, as is experimentally

observed. The *ab initio* determined energetics associated with the vacancy diffusion will used as input for Kinetic Monte Carlo calculations to study void growth by vacancy condensation.

A lattice Kinetic Monte Carlo (KMC) simulation will be set up [44] to determine the key aspects of vacancy motion and void nucleation. In this simulation, we first introduce a model for vacancy jump frequencies in which we account for the influence of the local stress, electron wind, and surface proximity on the migration energy barrier [45,46]. Generated vacancies will jump on an fcc lattice, and will interact at close distances according to the Embedded Atom Potential (EAM). Thus, the nucleation rates of small vacancy clusters will be accurately determined, since classical nucleation theory gives only qualitative information on void nucleation [47,48]. The local atomic jump rates of vacancies within a small cluster in a crystal region where stress, electron wind and surface proximity influence the saddle point energies will be employed to determine the general drift motion of nano-voids, their coalescence and eventual growth into larger voids.

Incorporation of elasticity, electron scattering, ab intio and empirical energetics into the KMC model should give accurate information on the initial phases of void nucleation and growth. However, the long-term behavior and growth of larger voids cannot be easily simulated by KMC because of computational limitations, even with large-scale computing capabilities, such as what we have at UCLA. To gain materials-design oriented information at larger length scales, we will develop a phase field model for void growth. The model includes spatially dependent rate equations for vacancy transport, vacancy cluster nucleation, motion and coalescence, and finally void growth [49,50]. The model will incorporate the information gained from lower length scales on vacancy energetics, sources and migration, and vacancy cluster nucleation. The resulting set of PDE's will be solved first in 2-D on a Voronoi tessellated triangular mesh. Based on these results, the need for extension to 3-D solution of the phase field model will be assessed, and if determined to be necessary, a 3-D extension will be made.

Research Timeline:

YEAR 1:

- Electroplating and mechanical behavior of nano-twinned Cu
- Synthesis and sintering of hollow SiO_2 nanoshells
- Ab initio calculations of Multiplane generalized stacking fault energy surfaces
- Stacking fault energy surfaces for twin boundaries
- Extension of the Peierls Nabarro model to twin boundaries
- MD simulations of twinning and de-twinning at the nano-scale
- KMC modeling of vacancy transport, clustering and void nucleation

YEAR 2:

- Electroplating and mechanical behavior of nano-twinned Cu
- Synthesis and sintering of hollow SiO_2 nanoshells
- Deposition and explosive reaction of nanolayer thin film UBM
- In-Situ electromigration experiment in TEM
- Extension of the Peierls Nabarro model to twin boundaries (continuation)
- Hybrid continuum-atomistic model for 3D dislocation loops in twin boundaries
- Molecular Dynamics based on empirical potentials for interactions of dislocations with twin boundaries
- Dislocation Dynamics Simulations of twins
- KMC modeling of vacancy transport, clustering and void nucleation (continuation)

YEAR 3:

- Electroplating and mechanical behavior of nano-twinned Cu
- Synthesis and sintering of hollow SiO_2 nanoshells
- Deposition and explosive reaction of nanolayer thin film UBM

- In-Situ electromigration experiment in TEM
- Ab initio electronic structure calculations to investigate the energy release during the formation of the multiplayer Al/Ni
- Ab initio studies for the effects of Sn and Si_3N_4 overlayers; Adhesion properties of multilayers
- Develop codes for electromigration wind force on dislocations and twin boundaries
- Dislocation Dynamics simulations of collective dislocation-twin boundary motion and nano-scale plasticity.
- Phase Field modeling of nano-voids in twinned Cu

YEAR 4:

- Deposition and explosive reaction of nanolayer thin film UBM
- In-Situ electromigration experiment in TEM
- Apply the codes developed in Year 3 to study the electromigration properties of dislocations and twin boundaries, and the effect of the Sn, Si_3N_4 and refractory interfaces on electromigration properties
- Ab intio calculations for vacancy formation and migration energetics of the Cu/Sn interface.
- Phase Field modeling of nano-voids in twinned Cu (continuation)
- Predictive modeling of degradation and reliability.

C.IV. Management, Education and Outreach

Management

Professors King-Ning Tu and nasr Ghoniem at UCLA will serve as the managing PI and associate managing PI of this project, respectively. Professor Tu will be in charge of coordinating research activities with the other three co-PIs from UCLA and California State University Northridge. He will also be responsible for making arrangements for networking, exchanging and disseminating the data and results with industrial partners. A regular joint group meeting will be held monthly to allow the students and postdocs to present the research progress, exchange information and plan future research activities.

Education

The fundamental goal of this collaborative project is to advance scientific innovation in nanostructured materials for interconnect and packaging technology, while providing training for undergraduate, graduate students and postdoctoral scholars. The PIs maintain a long standing commitment to the integration of research and education. The true foundation of collaborative scholarship and discovery, however, comes from the talented and motivated team of students and postdoctoral scholars that carry out the research. We anticipate using the NSF budget to support four graduate students and 1.5 postdoctoral scholars each year.

To integrate education and research, we will develop two graduate courses at UCLA on " Mechanical properties of Nanoscale structures" and "Kinetic processes in nanoscale structures." The Kinetic Processes in Nanoscale Structures will cover the following topics: 1. Theory of atomic diffusion in solids (8 hrs), 2. Planar and curved surfaces and Gibbs-Thomson potential (2 hrs),3. Nano wire growth in macro-pores of Si and AAO (2hrs), 4. VLS-model of growth of nano-Si wires (2 hrs), 5. Solid phase epitaxial growth of nano Si wires on silicide particles (2 hrs), 6. Interdiffusion in man-made superlattices of nano-scale periodicity (8 hrs), 7. Ham's model of precipitation and LSW theory of ripening (8 hrs), 8. Growth of hollow nano-spheres by nano Kirkendall effect (4 hrs), and 9. Self-organized growth of nano dots and wires on Si surfaces (4 hrs). The Mechanical Properties of Nanoscale Structures will cover the following topics: (1) Computational quantum mechanics (6 hrs); (2) Atomic bonding & interatomic potentials (4 hrs); (3) Computational Molecular Dynamics (MD) (5 hrs); (4) Monte Carlo Methods (4 hrs); (5) Mechanics of Defects (8 hrs); (6) Dynamical Properties & Phonons (5 hrs); (7) Mechanical Behavior at the Nano-scale (8 hrs). Professor Ghoniem was invited by NSF to give a "short course" with

similar topics at the South America Workshop on Advanced Materials, Rio de Janiero, Brazil, during August 2004.

In addition, we plan to have a series of short courses on these topics through UCLA extension to train engineers working in the microelectronics industry.

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